Kindly amend the claims without prejudice, as follows:

Cancel claims 1-3, 5, 6, 10-14 and 17-29, without prejudice.

Add claims 30 – 45.

Note that claims: 4, 7-9, 15, and 16 were previously canceled.

LISTING OF CLAIMS:

1. (Canceled)
2. (Canceled)
3. (Canceled)
4. (Previously canceled)
5. (Canceled)
6. (Canceled)
7. (Previously canceled)
8. (Previously canceled)
9. (Previously canceled)
10. (Canceled)
11. (Canceled)
12. (Canceled)
13. (Canceled)
14. (Canceled)
15. (Previously canceled)
16. (Previously canceled)
17. (Canceled)
18. (Canceled)
19. (Canceled)
20. (Canceled)
21. (Canceled)
22. (Canceled)
23. (Canceled)
24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (Canceled)

29. (Canceled

30. (New) A dual loop synchronization system comprising:

a phase lock loop (PLL) having a phase/frequency detector (PFD), a voltage controlled oscillator (VCO), and a phase shifter coupled to said VCO configured in a feedback loop with said PFD, and receiving a local reference clock signal;

a first-in first-out (FIFO) register receiving a parallel data input; and

a delayed lock loop (DLL) having a detector coupled to the output of said FIFO register for detecting the fill level of said FIFO and a digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PLL.

31. (New) A dual loop synchronization system as in claim 30, wherein said PLL is embedded within the DLL:

32. (New) A dual loop synchronization system as in claim 30, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO is a phase detector.

33. (New) A dual loop synchronization system as in claim 32, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO is a binary phase detector.

34. (New) A dual loop synchronization system as in claim 33, wherein said detector coupled to the output of said FIFO register for detecting the fill level of said FIFO is a wide band phase detector.

35. (New) A dual loop synchronization system as in claim 30, wherein said PLL further comprises:

a loop filter coupled between sad PFD and said VCO.

36. (New) A dual loop synchronization system as in claim 35, wherein the loop filter coupled between sad PFD and said VCO is configured as a wide bandwidth loop for suppressing VCO phase noise.

37. (New) A dual loop synchronization system as in claim 30, wherein said digital loop filter coupled between said detector and said phase shifter of said PLL to produce a phase shift in said PL is a narrow bandwidth filter.

38. (New) A dual loop synchronization system as in claim 30, further comprising:

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register; and

a comparison module receiving and output signal from both said write counter and said read counter.

39. (New) A dual loop synchronization system as in claim 30, further comprising:

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a reset counter receiving an input signal from both said write counter and said read counter; and

a register receiving an input signal from both said reset counter and said read counter.

40. (New) A dual loop synchronization system as in claim 30, further comprising:

a write counter receiving a write clock signal and providing an output to said FIFO register;

a read counter receiving a read clock signal and providing an output to said FIFO register;

a binary decoder; and

a plurality of phase detectors receiving an input from said counters and said FIFO register and also providing an output to said FIFO register and said binary decoder.

41. (New) A method for data synchronization in a plesiochronous system comprising the steps of:

receiving write data in a FIFO;

detecting the fill level of the FIFO at the input of a DLL;

providing a signal based on the detected fill level to a PLL;

receiving a local reference clock signal in the PLL;

shifting the phase of the local reference clock signal in the PLL in response to the signal based on the detected fill level provided by the DLL.

42. (New) A method for data synchronization in a plesiochronous system as in claim 40, further comprising:

filtering the signal based on the detected fill level in the DLL before providing it to the PLL.

43. (New) A method for data synchronization in a plesiochronous system as in claim 42, wherein the step of filtering is performed with a narrow bandwidth filter.

44. (New) A method for data synchronization in a plesiochronous system as in claim 40, wherein in the step of receiving a local reference clock signal in the PLL, the local reference clock is received at a phase/frequency detector in the PLL and further comprising:

filtering a signal at the output of the phase/frequency detector in a loop filter; and

providing the output of the loop filter to a VCO.

45. (New) A method for data synchronization in a plesiochronous system as in claim 44, wherein the step of filtering is performed in a wide bandwidth filter.